Thermoelectric performance of silicon nanowires

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With finite element simulation and analytic modeling, the thermoelectric performance of silicon nanowires (SiNWs) is studied. Large cooling temperature is observed which increases remarkably as thermal conductivity of SiNW decreases. Moreover, high cooling power density of 6.6 \times 10^3 W/cm² is achieved which is about 600 times larger than that of commercial thermoelectric modules. Moreover, SiNW cooler can reach the coefficient as high as 61%. All these features make SiNW a very promising material in application of on-chip temperature controlling and heat dissipating for hot spots inside integrated circuits. © 2009 American Institute of Physics.

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In existing microelectronic devices, hot spot removal is a key for future generation integrated circuit chips.1 Thermoelectric (TE) module is one of current available cooling technologies. In the nanoscale TE materials, silicon nanowires (SiNWs) are of crucial importance.2,3 For a good TE material, the material must have a high figure of merit (ZT), which is proportional to the Seebeck coefficient (S), electrical conductivity, and absolute temperature, but inversely proportional to thermal conductivity. In SiNWs, the electrical conductivity and Seebeck coefficient are similar to those of bulk silicon, but exhibit 100-fold reduction in thermal conductivity.4–7 Recent experiments8,9 have provided direct evidence that an approximately 100-fold improvement of the ZT values over bulk Si is achieved in SiNW. A natural question comes promptly: if a cooler is built from SiNW, then how cool can we achieve? Also, what are the cooling power and efficiency? In this letter, we will answer these questions through investigations with finite element simulation and analytic modeling.

One-dimensional structures have obviously different thermal properties from bulk material. For instance, in a carbon nanotube, heat conduction does not obey the Fourier law.10–12 However, it has been demonstrated that using classical transport model can describe the thermal property of nanostructured silicon system correctly.13–15 We perform numerical simulation based upon macro scale heat transfer models with experimental reported material properties.

Our simulations are based on a model that the SiNW is in contact with a silicon island (both are suspended). The size of SiNW is 50 nm \times 50 nm \times 2.5 \mu m and the size of the silicon island is 20 \mu m \times 20 \mu m \times 200 nm. Upon electrical current flow through, Peltier effect can create a cold and hot side. Here the silicon island is in contact with the cold side and the hot side is fixed at 300 K. Besides Peltier effect, the reverse flow of heat from hot end to cold end and Joule heat will weaken the cooling efficiency. In our model, heat flux is the sum of Seebeck (Peltier) effect, Fourier effects, and the Joule heat. The governing equation which represents the heat transfer is

\[
\nabla \cdot (-k \cdot \nabla T + S \cdot T \cdot J) = J \cdot (-\nabla \cdot V) - c \frac{\partial T}{\partial t},
\]

where \(k\), \(S\), and \(T\) are the thermal conductivity, the Seebeck coefficient, and the temperature, respectively. \(c\) is the thermal capacity. \(J\) and \(V\) are the applied electrical current density and the electrostatic potential, respectively. We only consider the steady-state case, thus \(\partial T/\partial t = 0\). In our simulations, the Seebeck coefficient and electrical resistivity of SiNW are 245 \mu V/K and 1.7 \times 10^{-5} \Omega m at 300 K, respectively, which are similar to those of bulk Si with the same doping concentration.9 For SiNW with 50 nm diameter, 20 W/m K is observed for vapor-liquid-solid (VLS)-grown SiNW, while 1.6 W/m K is found for aqueous electronless-etching (EE)-grown wire.5,8 In our simulations, both thermal conductivity values are used. For simplicity, these two types of SiNWs are named as VLS-SiNWs and EE-SiNWs, respectively.

Natural convection and radiation as the heat transfer mechanism between the system and the surrounding air are established.15,16 The finite element modeling is used to perform a steady-state thermal analysis to evaluate temperature profile. We employed COMSOL MULTIPHYSICS,17 a finite element program, to simulate the cooling temperature, cooling power density, and coefficient of performance (COP).

Figure 1(a) shows the temperature profile along the SiNW with electrical current of 3.5 \mu A. A temperature decrease of about 60 K is observed. Figure 1(b) shows the temperature distribution along the SiNW if the wire is VLS wire. With current up to 9 \mu A, the Joule heat increases, and the net cooling is reduced. Under this current, the central temperature of the wire is higher than those of the two ends, as shown in Fig. 1(c). From Fig. 1(d), it is obvious that SiNW with low thermal conductivity benefits the TE performance remarkably.

Figure 2 shows the cooling temperature versus electrical current. For both EE and VLS wires, the cooling temperature increases with supplied current increases and there is a maxi-
imum at about $I_M = 3.5 - 4.0 \ \mu A$. Above $I_M$, cooling temperature decreases with increasing current. This phenomenon can be understood as below. Increasing electrical current has two effects on cooling. On the one hand, the increase of electrical current will absorb more thermal energy from one end and transport it to another end. We call this effect the “positive” effect. On the other hand, the increase of electrical current will also increase Joule heating that in turn will increase the heat flux to the cool end, thus suppress cooling. We call it the “negative” effect. The cooling temperature is determined by these two effects that compete with each other.

In the cooling temperature calculation above, the silicon island is a nonsource device. If the device (silicon island) generates heat, the maximum cooling temperature will depend on the dissipation power and we can predict the maximum cooling power that SiNW cooler can achieve. Figure 3 shows the relation between the cooling temperatures with the power dissipation density from the device for both EE- and VLS-SiNWs. The maximum cooling power density is defined as the heat load power that makes the device’s maximum cooling temperature equal to zero. The maximum cooling power density is about $6.6 \times 10^3 \ \text{W/cm}^2$ here and is independent on the special thermal conductivity. The maximum cooling power density $6.6 \times 10^3 \ \text{W/cm}^2$ for SiNW, is about six times larger than that of SiGeC/Si superlattice coolers, ten times larger than that of Si/Si$_x$Ge$_{1-x}$ thin film cooler, and 600 times larger than that of commercial TE module.

The performance of TE material is in general expressed by its COP. This is defined as the actual cooling power divided by the total rate at which electrical energy is supplied. From Fig. 3, we can obtain the COP for SiNWs are $61\%$. This is larger than that of Si/Si$_x$Ge$_{1-x}$ thin film cooler, which is $36\%$, and larger than that of commercial TE module which is only $0.1\%$. In the following, we will explore the cooling temperature with analytical equations. The cooling effect at the junction is opposed by Joule heat in the nanowire and by heat conducted from the hot end. We assume that half of Joule heat travels to each of the ends. Neglecting the heat radiation.
between the device and the surrounding air, the rate of absorption of heat from the source is given by
\[ Q_{ab} = S T c I - \frac{1}{2} f^2 R - \frac{A}{L} (T_H - T_c). \] (2)

Then the maximum cooling temperature is given by
\[ \Delta T = \frac{STcI - \frac{1}{2} f^2 R}{SI + \frac{A}{L}}. \] (3)

Here \( R, L, \) and \( A \) are the electrical resistance, the length, and the cross-section area of the SiNW. Figure 2 shows the cooling temperature versus electric current curves calculated from the analytical expression. They are in good agreement with those obtained from finite element calculations.

From the analytical expression of cooling temperature, we can provide a prediction of the transverse size effect on the cooling temperature. As the thermal conductivity of EE wire depends on both the transverse dimension and the surface roughness, and the accurate quantitative relation between thermal conductivity and surface roughness is not clear, here we only show the results of VLS wires. For SiNWs with length in micrometer scale, the thermal conductivity increases with diameter increases remarkably.\(^{21-23}\) The quantitative formula for the diameter-dependent thermal conductivity of SiNW is
\[ \frac{\kappa}{\kappa_b} = p \exp \left( - \frac{d_b}{D} \right) \left( \exp \left( - \frac{(\alpha - 1)}{D / \alpha - 1} \right) \right)^{3/2}. \] (4)

Here \( \kappa \) is the thermal conductivity of SiNW and \( \kappa_b \) is the thermal conductivity of bulk silicon. The details about this formula can be found in Ref. 21. Figure 4(b) shows the cooling temperature versus electrical current for SiNWs with different diameters. It is obvious that cooling temperature decreases as diameter increases, and the electrical current \( I_M \), at which the cooling temperature reaches the maximum value, increases with diameter. When the diameter increases to 100 nm, the maximum cooling temperature is only about 4 K, as shown in Fig. 4(c). So to keep high cooling temperature, SiNW with small diameter is preferred. Here we focus on the steady state analysis, so the cooling performance is independent on the size (or thermal capacity) of the silicon island. In practical application, a bundle of SiNWs can be used to generate larger cooling power and faster cooling response.

In conclusion, with finite element simulation and analytic modeling, we have studied the TE performance of SiNWs. Large cooling temperature has been achieved. Moreover, high cooling power density of \( 6.6 \times 10^3 \) W/cm\(^2\) has been also obtained. We have compared the performance of SiNW cooler with that of the current most used commercial TE modules and the silicon based superlattice coolers, to strengthen its advantages as nanoscale cooler. Our results have demonstrated that SiNW has a great potential in application in on-chip temperature cooling and hot spots removing in integrated circuits.

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